REMARKS

Claims 1 to 8, 10 to 18 and 20 to 30 are pending this application of which claims 1, 11 and 21 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Claims 1 to 8, 10 to 18 and 20 to 30 were rejected under 35 U.S.C. § 102 over Rostoker et al. (U.S. Patent No. 5,544,067). As shown above, Applicants have amended the claims to define the invention more clearly. In view of these amendments, withdrawal of the art rejection is respectfully requested.

Claim 1, as amended, is directed to a method of generating a logic design for use in designing an integrated circuit (IC). The method includes embedding a computer instruction representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design. The two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD).

The applied art is not understood to disclose or suggest the foregoing features of claim 1. In particular, Rostoker does not disclose or suggest "embedding a computer instruction representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design."

Specifically, Rostoker discloses combinatorial computer instructions separate from a two-dimensional schematic representation (FIGS. 13 to 15 of Rostoker). Rostoker shows a different display window for each representation (i.e., one window for computer instructions, one window for a block diagram, and so forth).

The Examiner has indicated that FIG. 18 of Rostoker is an example of embedding a computer instruction in a two-dimensional schematic representation. Applicants disagree. Fig 18 of Rostoker shows circuit elements, namely flip-flops and a NOR gate, together with a state table showing states of the various circuit elements. No computer instructions are shown. Therefore, Rostoker does not disclose or suggest "embedding a computer instruction representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design." Accordingly, Applicants respectfully request removal of this art rejection.

Claims 1 to 8, 10 to 18 and 20 to 30 were rejected under 35 U.S.C. § 102(b) for a public use or sale of the Mentor Graphics Renoir tool that uses HDL2Graphics based on the Mentor Graphics data sheets (HDL Design data sheet and Renoir with HDL2Graphics data sheet).

Initially, Applicants note that the cited data sheets do not constitute a public disclosure of Applicants' invention. The cited data sheets references Mentor Graphics product, not an Intel product (the assignee of the subject application).

The rejection over the Mentor Graphics data sheets will be addressed as an ordinary §102(b) rejection as follows. The Mentor Graphics data sheets do not disclose or suggest "embedding a computer instruction representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design."

The Mentor Graphics datasheets indicate that computer instructions and two-dimensional schematic representations may be used to design an IC, but the datasheets do disclose or suggest

that the computer instructions of a combinatorial block are embedded into the two-dimensional representations. Moreover, the datasheets show each of the representations in separate display windows. For example, the first page of the HDL Design data sheet shows one display window for code and a second display window for combinatorial blocks. In another example, the Renoir with HDL2Graphics data sheet shows different display windows and indicates that the design tool can convert VHDL and Verilog to graphics. However, nowhere in the data sheet is it disclosed or suggested "embedding a computer instruction representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design." Accordingly, Applicants respectfully request withdrawal of this rejection.

Claims 11 and 21 roughly correspond to claim 1. Accordingly, claims 11 and 21 are believed to be allowable for at least the same reasons noted above with respect to claim 1.

Finally, the Examiner has requested a copy of the Renoir User's manual. Applicants' attorneys have tried, but have been unable, to obtain a copy of the manual, since, as noted, the product described therein is not manufactured by Intel. Applicants respectfully request withdrawal of this requirement.

In view of the foregoing amendments and remarks, Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the below address. Applicants' attorney can be reached by telephone at the number shown below.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 10559-595001.

Respectfully submitted,

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Paul A. Rysher
Reg. No. 40,780

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

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